In the Claims:

1. (Currently amended) A method for producing a semiconductor device having ~~and using~~ an alignment mark, the method comprising the steps of:

forming a first dielectric layer;

etching a trench having predetermined dimensions into the dielectric layer;

depositing a first layer of metal into the trench;

forming a second dielectric layer over the first dielectric layer and over the first layer of metal;

depositing a first resist layer over said second dielectric layer;

patterning said first resist layer to define a first multiplicity of apertures and an array of openings, said array of openings having a predetermined periodicity and each opening having a selected width;

etching, simultaneously, said first multiplicity of apertures and said array of openings ~~channels and an opening~~ into the second dielectric layer a first distance;

depositing a second resist layer over said etched second dielectric layer;

patterning said second resist layer to define a second multiplicity of apertures;

etching said second multiplicity of apertures a second distance, ~~at least one of the channels used as a via extending to the first layer of metal and the opening extending through the second dielectric layer whereby a bottom surface of the opening is coplanar to a top surface of the first metal layer;~~

filling the apertures ~~channels~~ and the array of openings ~~opening~~ with a metal ~~and plating a remaining portion of the surface of the second dielectric layer with metal~~, the filling step controlled to fill the channels and under fill the array of openings ~~opening~~, said selected width of said openings being at least two times the depth of said openings;

performing chemical mechanical polishing of the metal; and

depositing a non-transparent stack of layers onto the metal to cover ~~and the remaining portions of a top surface of the second dielectric layer, whereby the non-transparent stack of layers conforms to the surface of~~ the under filled array of openings ~~opening~~, resulting in an

alignment ~~mark on~~ grating comprised of visible indentations in the non-transparent stack of layers.

2. (Original) The method of Claim 1 wherein the semiconductor device is a Magnetoresistive Random Access Memory.

3. (Original) The method of Claim 1 wherein the semiconductor device is a metal-insulator-metal capacitor.

4. (Original) The method of Claim 1 wherein the formation of the first and second dielectric layers is performed through chemical vapor deposition.

5. (Original) The method of Claim 4 wherein the chemical vapor deposition is plasma enhanced chemical vapor deposition.

6. (Currently amended) The method of Claim 1 wherein the etching of the trench, and the first and second multiplicity of apertures ~~channels~~ and array of openings ~~opening~~ is performed through Reactive Ion Etching.

7. (Original) The method of Claim 1 wherein the first and second dielectric layers are comprised of a low constant dielectric material.

8. (Original) The method of Claim 7 wherein the low constant dielectric material is chosen from the group consisting of silk, fluorinated oxide, and silicon dioxide.

9. (Currently amended) The method of Claim 1 wherein the metal used for filling ~~and plating~~ is ~~comprised of~~ copper.

10. (Currently amended) The method of Claim 1 wherein the step of filling comprises:

depositing a liner layer into the first and second multiplicity of apertures ~~channels~~ and the array of openings ~~opening~~; and

depositing a metal onto the liner layer.

11. (Currently Amended) The method of Claim 10 wherein the liner layer is comprised of tantalum ~~tantelum~~.

12. (Original) The method of Claim 10 wherein the liner layer is comprised of tungsten nitride.

13. (Original) The method of Claim 1 wherein the plating metal thickness is about 7500 to about 8500 angstroms.

14-21 (Canceled)

22. (New) The method of Claim 1 wherein said first etch distance is less than the thickness of said second dielectric layer and said second resist layer is patterned such that at least one of said second apertures is defined directly over one of said apertures of said first multiplicity of apertures such that etching said at least one aperture of said second multiplicity of apertures forms a via through the remainder of said second dielectric layer to contact said first layer of metal in said trench.

23. (New) The method of Claim 1 wherein said first multiplicity of apertures are located directly over said first layer of metal and said first etch distance extends through said second dielectric layer and forms vias to said first layer of metal and said second etch distance is less

than said first etch distance such that said second multiplicity of apertures do not extend through said second layer of dielectric.

24. (New) The method of Claim 1 wherein said first multiplicity of apertures are located directly over said first layer of metal and said first etch distance extends through said second dielectric layer and forms vias to said first layer of metal, and said defined second multiplicity of apertures including a first group of apertures and a second group of apertures, said second group being said array of openings such that etching said first group of apertures forms channels that extend less than the thickness of said second dielectric layer and etching said second group of apertures results in said array of openings extending through said second dielectric layer and into said first dielectric layer.